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DATE: February 17, 2006

FROM: Trevor Lind

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RE: Application Serial No. 09/640,802

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☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) 500.00

Complete if Known

Application Number	09/640,802
Filing Date	August 17, 2000
First Named Inventor	Tai Anh Cao et al.
Examiner Name	Ted M. Wang
Art Unit	2634
Attorney Docket No.	AUS9-2000-0285-US1

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Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180
Total Claims	Extra Claims	Fee (\$)
- 20 or HP = _____ x _____ = _____		
HP = highest number of total claims paid for, if greater than 20.		
Indep. Claims	Extra Claims	Fee (\$)
- 3 or HP = _____ x _____ = _____		
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PATENT
AUS9-2000-0285-US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:)
Tai Anh Cao et al.)
Serial No.: 09/640,802) Group Art Unit: 2634
Filed: August 17, 2000)
FOR: CIRCUIT FOR FACILITATING) Examiner: Ted M. Wang
SIMULTANEOUS MULTI-)
DIRECTIONAL TRANSMISSION)
OF MULTIPLE SIGNALS)
BETWEEN MULTIPLE CIRCUITS) Facsimile No.: (571) 273-8300
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APPEAL BRIEF

This is an appeal from the Final Office Action mailed September 20, 2005 (the "Final Office Action"), rejecting claims 5, 6, 11, 12, 15, and 16. Appellants submit this Appeal Brief to the Board of Patent Appeals and Interferences within the two-month period following the Notice of Appeal filed December 20, 2005.

This Appeal Brief is accompanied by an authorization (Fee Transmittal form PTO/SB/17) to charge Deposit Account No: 09-0447 for the fee of \$500.00 due under 37 C.F.R. §41.20(b)(2), together with any additional fees which may be required for filing this Appeal Brief.

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I. REAL PARTY IN INTEREST (37 C.F.R. §41.37(c)(1)(i))

The above-described patent application is assigned to International Business Machines Corporation ("IBM"), the real party in interest.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. §41.37(c)(1)(ii))

There is no related Appeal or Interference before the United States Patent and Trademark Office.

III. STATUS OF THE CLAIMS (37 C.F.R. §41.37(c)(1)(iii))

The status of the claims is as follows:

Allowed Claims: 1 through 4, 7 through 10, 13, 14, and 18

Claims to which Objections apply: None

Claims withdrawn from consideration: None

Claims Rejected: 5, 6, 11, 12, 15, and 16

Claims Appealed: 5, 6, 11, 12, 15, and 16

IV. STATUS OF AMENDMENTS (37 C.F.R. §41.37(c)(1)(iv))

The amendments to the specification filed December 20, 2005, in response to the Examiner's comments and objections in the November 14, 2005 Advisory Action have been entered as indicated by the Advisory Action mailed January 17, 2006.

1 No amendments to the claims have been filed subsequent to the September 20, 2005 Final
2 Office Action. The claims reproduced in the accompanying Claims Appendix reflect the state of
3 the claims as they currently stand in this case.
4

5 **V. SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. §41.37(c)(1)(v))**

6 The present invention includes an electronic circuit 104 adapted to send a signal to two or
7 more separate electronic circuits 105 and 106 over a common transmission line 108 while
8 simultaneously receiving signals from the two or more separate electronic circuits 105 and 106
9 over the common transmission line 108 (p. 7, lines 6-13). The electronic circuit 104 includes
10 signal sending circuitry coupled to an interface node 117 which is adapted to be coupled to the
11 common transmission line 108 (p. 7, lines 24-26; p. 8, lines 5-7). The signal sending circuitry
12 creates a combined signal at the interface node 117 (p. 11, lines 21-23). This combined signal is
13 dependent on the signal from the electronic circuit 104 and the signals simultaneously applied by
14 the two or more separate electronic circuits 105 and 106 connected at other points 118 and 119 to
15 the common transmission line 108 (p. 10, line 24 - p. 11, line 2; p. 8, lines 7-9). The electronic
16 circuit 104 also includes decoding circuitry 110 coupled to the interface node 117 (p. 7, line 26 -
17 p. 8, line 7). This decoding circuitry 110 detects the combined signal at the interface node 117
18 and decodes the signals from the two or more separate electronic circuits responsive to the
19 combined signal (p. 9 lines 5-20; p. 7, line 26 - p. 8, line 7).

20 The present invention also includes an electronic circuit arrangement 100 including three
21 or more circuits 104, 105, and 106 connected together by a common transmission line 108, where
22 each circuit 104, 105, and 106 is adapted to assert a respective digital signal (p. 7, lines 6-13).

1 Each circuit 104, 105, and 106 includes respective sending circuitry connected to the common
2 transmission line 108 and this sending circuitry cooperates to produce an encoded signal on the
3 transmission line 108 based upon the values of the respective digital signals asserted by the
4 respective circuits 104, 105, and 106 (p. 7, line 24 - p. 8, line 9; p. 10, line 24 - p. 11, line 2).
5 The encoded signal comprises one signal from a set of unique encoded signals. Each different
6 signal in the set of encoded signals is representative of a particular combination of digital signals
7 asserted simultaneously from the respective circuits 104, 105, and 106 (p. 11, lines 21-23). Each
8 circuit 104, 105, and 106 also includes a respective decoding arrangement 110, 112, and 114 for
9 decoding the encoded signal appearing on the common transmission line 108 to produce the
10 digital signals asserted from each other circuit 104, 105, and 106 (p. 8, lines 14-23).
11

12 Means Plus Function Expressions

13 Claim 1 elements (a) and (b), claim 7 elements (b) and (c), and claim 13 elements (a) and
14 (b) include means plus function expressions under 35 U.S.C. 112, paragraph six.
15

16 Claim 1

17 Claim 1 element (a) includes the means plus function expression, "...the signal sending
18 circuitry creating a combined signal at the interface node." The structure of the signal sending
19 circuitry of element (a) includes a DRIVER A and encoding element 109 for circuit 104,
20 DRIVER B and encoding element 111 for circuit 105, and DRIVER C and encoding element 113
21 for circuit 106 (Figures 1-4 and p. 7, line 24 - p. 8, line 5). The encoding elements 109, 111, and

1 113 are shown as resistors Ra, Rb, Rc, respectively, in Figures 2, 3 and 4 (p. 8, line 26 - p. 9, line
2 3).

3 Element (b) of claim 1 includes the means plus function expression, "...the decoding
4 circuitry detecting the combined signal at the interface node and decoding the signals from the
5 two or more separate electronic circuits responsive to the combined signal." Figure 1 shows the
6 decoding circuitry at 110 for circuit 104, at 112 for circuit 105, and at 114 for circuit 106 (p. 7,
7 line 26 - p. 8, line 5). Figure 2 shows a particular decoding circuit 110 made up of a second
8 signal decoding arrangement 201 and a third signal decoding arrangement 204 (p. 9, lines 5-20).
9 Figure 3 shows a particular decoding circuit 112 made up of a first signal decoding arrangement
10 301 and a third signal decoding arrangement 303 (p. 9, line 21 - p. 10, line 8). Figure 4 shows a
11 particular decoding circuit 114 made up of a first signal decoding arrangement 401 and a second
12 signal decoding arrangement 403 (p. 10, lines 9-23).

13
14 Claim 7

15 Claim 7 element (b) includes the means plus function expression, "...the sending circuitry
16 of the respective circuits cooperating to produce an encoded signal on the transmission line based
17 upon the values of the respective digital signals asserted by the respective circuits." The
18 structure of the sending circuitry of element (b) includes a DRIVER A and encoding element 109
19 for circuit 104, DRIVER B and encoding element 111 for circuit 105, DRIVER C and encoding
20 element 113 for circuit 106 (Figures 1-4 and p. 7, line 24 - p. 8, line 5). The digital signal
21 encoding elements 109, 111, and 113 are resistors Ra, Rb, Rc, respectively, in Figures 2, 3, and 4
22 (p. 8, line 26 - p. 9, line 3).

1 Claim 7 element (c) includes the means plus function expression, "...a decoding
2 arrangement for decoding the encoded signal appearing on the common transmission line to
3 produce the digital signals asserted from each other circuit." Figure 1 shows the decoding
4 circuitry at 110 for circuit 104, at 112 for circuit 105, and at 114 for circuit 106 (p. 7, line 26 - p.
5 8, line 5). Figure 2 shows a particular decoding circuit 110 made up of a second signal decoding
6 arrangement 201 and a third signal decoding arrangement 204 (p. 9, lines 5-20). Figure 3 shows
7 a particular decoding circuit 112 made up of a first signal decoding arrangement 301 and a third
8 signal decoding arrangement 303 (p. 9, line 21 - p. 10, line 8). Figure 4 shows a particular
9 decoding circuit 114 made up of a first signal decoding arrangement 401 and a second signal
10 decoding arrangement 403 (p. 10, lines 9-23).

11
12 Claim 13

13 Claim 13 element (a) includes the means plus function expression, "...the first, second,
14 and third encoding elements cooperating to produce an encoded signal on the common
15 transmission network based upon the values of the first, second, and third digital signals." The
16 first, second, and third encoding elements 109, 111, and 113 are resistors Ra, Rb, Rc,
17 respectively, in Figures 2, 3, and 4 (p. 8, line 26 - p. 9, line 3).

18 Element (b) of claim 13 includes the means plus function expression, "...the respective
19 decoding arrangement for each respective circuit for decoding the encoded signal to produce the
20 digital signals produced by each other circuit in the system." Figure 1 shows the decoding
21 circuitry at 110 for circuit 104, at 112 for circuit 105, and at 114 for circuit 106 (p. 7, line 26 - p.
22 8, line 5). Figure 2 shows a particular decoding circuit 110 made up of a second signal decoding

1 arrangement 201 and a third signal decoding arrangement 204 (p. 9, lines 5-20). Figure 3 shows
2 a particular decoding circuit 112 made up of a first signal decoding arrangement 301 and a third
3 signal decoding arrangement 303 (p. 9, line 21 - p. 10, line 8). Figure 4 shows a particular
4 decoding circuit 114 made up of a first signal decoding arrangement 401 and a second signal
5 decoding arrangement 403 (p. 10, lines 9-23).

6
7 **VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**
8 **(37 C.F.R. §41.37(c)(1)(vi))**
9

10 Claims 5, 6, 11, 12, 15, and 16 stand rejected under 35 U.S.C. §112, second paragraph, as
11 being indefinite for failing to particularly point out and distinctly claim the subject matter of the
12 present invention.

13
14 **VII. ARGUMENT (37 C.F.R. §41.37(c)(vii))**

15 **CLAIMS 5, 6, 11, 12, 15, AND 16 ARE NOT INDEFINITE UNDER 35 U.S.C. §112, SECOND**
16 **PARAGRAPH**

17 The Final Office Action rejected claims 5, 6, 11, 12, 15, and 16 under 35 U.S.C. §112,
18 second paragraph as being indefinite for failing to particularly point out and distinctly claim the
19 subject matter of the invention. The Appellants believe this rejection under 35 U.S.C. §112,
20 second paragraph is in error.

21 All of the Section 112 rejections are made in view of designations in the claims such as
22 "a second differential receiver" where no "first" differential receiver had been previously
23 introduced in the claim or parent claim. (See Items 3-8 on pages 3-4 of the Final Office Action.)

1 The basis for each rejection is summed up in the Final Office Action at page 3, lines 6-10 as
2 follows:

3 A second differential receiver without introducing [sic] first differential receiver,
4 and a second and third reference voltage without introducing [sic] first voltage, for
5 example claim 5, make the [sic] claim 5 indefinite [sic] that there is insufficient
6 antecedent basis for the limitation in the claim.

7 There is No Lack of Antecedent Basis in the Rejected Claims

8 The Final Office Action appears to reject claims 5, 6, 11, 12, 15, and 16 based on lack of
9 antecedent basis solely in view of the use of a higher ordinal such as "a second element X" where
10 a "first element X" has not been previously referenced in the claim. However, a reference to "a
11 second element X" without any previous reference in the claim to "a first element X" simply
12 does not raise any antecedent basis issue. Rather, indefiniteness from a lack of antecedent basis
13 may arise in some cases when a definite article such as "the" is used to introduce an element for
14 the first time in a claim, or when a definite article is used to reference an element where two or
15 more of the same element have previously been referenced. In these cases it may be unclear as to
16 which particular element is being referenced in the claim. See M.P.E.P. §2173.05(e). However,
17 a reference to "a second element X" without any previous reference in the claim to "a first
18 element X" raises no issue regarding clarity as to the structure being claimed, particularly where
19 the claim language matches the language used to define elements in the disclosure, as it does in
20 this case. In addition, each of the currently rejected claims properly introduces each new
21 component with an indefinite article and references each previously introduced component with a
22 definite article. Thus, no antecedent basis issue arises in any of these claims. There is simply
23 never any issue as to which component is being referenced in the claims.

1 The Meaning and Scope of the Rejected Claims is Clear

2 The definiteness inquiry under 35 U.S.C. §112, second paragraph, is whether the claim
3 language makes the scope of the claim clear to a hypothetical person possessing the ordinary
4 level of skill in the pertinent art. M.P.E.P. §2171. If the claim language is such that the scope of
5 a claim would be reasonably ascertainable by those skilled in the art, then the claim is not
6 indefinite. *Ex parte Porter*, 25 USPQ2d 1144, 1145 (Bd. Pat. App. & Inter. 1992).
7 Furthermore, the definiteness of language employed in a claim must not be viewed in a
8 vacuum, but always in light of the application disclosure. *In re Moore and Janoski*, 169
9 U.S.P.Q. 236, 238 (C.C.P.A. 1971).

10 In this case, claims 5, 6, 11, 12, 15, and 16 are not indefinite. The meaning and scope of
11 each rejected claim is readily ascertainable simply by reference to the disclosure because the
12 same language used to name components in the claims is also used to reference components in
13 the disclosure. For example, claim 5 refers to "a reference voltage multiplexer connected to
14 receive a first digital signal as a control signal, and having second and third reference voltage
15 inputs" and further refers to "a second differential receiver having a positive input connected
16 to receive the combined signal, and a negative input connected to receive an output of the
17 reference voltage multiplexer." The second and third reference voltage inputs and the second
18 differential receiver referenced in claim 5 are first identified in the disclosure in the following
19 passage which begins at page 9, line 7 of the disclosure.

20 Decoding arrangement 201 includes reference voltage multiplexer 202 and second
21 differential receiver 203. Multiplexer 202 receives second and third reference
22 voltage inputs (V2 and V3) and is controlled by signal A to pass one of those
23 reference voltages to the negative input of second differential receiver 203.

1 All of the elements in this passage are shown in Figure 2.

2 Claims 6, 11, 12, 15, and 16 exhibit this same consistency between the terms used in
3 those claims and the terms used in the disclosure for the corresponding circuit components.
4 Therefore, the rejected claims in this case are not indefinite because the direct correspondence
5 between the claim language and the disclosure terminology makes the scope of these claims
6 perfectly clear.

7 The Manner in which Ordinals Appear in the Claims is a Natural Result of the Nature of the
8 Invention Being Claimed

9 The electronic circuit which is the subject of the present invention employs multiple
10 instances of certain components such as differential receivers, multiplexers, and reference
11 voltages. The Appellants have chosen to use ordinals (e.g., first, second, third, etc.) to
12 differentiate between similar components. For example, the disclosure refers to a "first
13 differential receiver 302," a "second differential receiver 203," and a "third differential receiver
14 206." In order to clearly and distinctly claim the subject matter which the Appellants regard as
15 the invention, the Appellants have chosen to maintain the same ordinals in the claims to
16 distinguish between components of the same type.

17 As shown in Figure 1 of the present application, three circuits are communicating with
18 each other that each have a respective decoding arrangement, 110, 112, or 114. As shown in
19 Figures 2 through 4, each of these decoding arrangements includes a specific decoding circuit for
20 decoding a respective signal from the combined signal. For example, Figure 2 shows a second
21 signal (signal B) decoding circuit 201, while Figure 3 shows a first signal (signal A) decoding
22 circuit 301. The dependent claims in this case are directed to the specific signal decoding circuits

1 and circuit decoding arrangements shown in Figures 2-4. In some cases, the dependent claims
2 are claiming circuits that do not include a "first" of one element, but do include a "second" or
3 some other higher ordinal of that element. For example, Claim 5 happens to claim the specific
4 second signal (signal B) decoding circuit shown at 201 in Figure 2. A comparison of decoding
5 circuit 201 and the first signal (signal A) decoding circuit 301 (Figure 3) reveals that circuit 201
6 does not include the element referenced as the first reference voltage V1. Thus, since claim 5 is
7 directed to decoding circuit 201, claim 5 does not describe a first reference voltage input, but
8 does refer to the second and third reference voltage inputs. Also, although decoding circuit 201
9 includes the second differential receiver 203, it does not require the component disclosed as the
10 first differential receiver, which is shown at 302 in Figure 3 and described in the disclosure at
11 page 9, lines 15-17. Thus, claim 5 refers to "a second differential receiver" but does not refer to
12 the first differential receiver.

13 Similarly to claim 5, claims 6, 11, 12, 15, and 16 are each directed to circuits that include
14 elements designated with higher ordinals in the disclosure (e.g. "a third differential receiver")
15 but do not include the elements designated with the corresponding lower ordinals (e.g. "a first
16 differential receiver" or "a second differential receiver"). As is the case with claim 5, the use of
17 ordinals in this manner is a natural result of the components of the respective decoding circuits
18 required by these claims in light of the overall structure of the present invention.

19 The use of ordinals in the claims as described above does not make the claims indefinite
20 under 35 U.S.C. §112, second paragraph because the meaning of claims 5, 6, 11, 12, 15, and 16
21 is not ambiguous and the language used in these claims clearly and precisely claims the subject
22 matter that the Appellants regard as the invention. The meaning and scope of each rejected claim

1 is readily ascertainable simply by reference to the disclosure because the same language used to
2 name components in the claims is also used to reference components in the disclosure. Thus, for
3 example, it is clear that the "second differential receiver" referenced in claim 5 refers to the
4 second differential receiver of the signal B decoding circuitry shown in Figures 2 and 4.
5 Therefore, since the scope of claims 5, 6, 11, 12, 15, and 16 is abundantly clear when considered
6 in view of the application disclosure and since there are no antecedent basis issues relating to the
7 rejected claims, these claims are by no means indefinite under 35 U.S.C. §112, second paragraph.

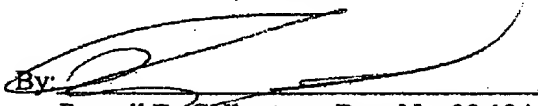
VIII. CONCLUSION

For all of the above reasons, the Appellants submit that claims 5, 6, 11, 12, 15, and 16 are entitled to allowance, and respectfully request that the Board reverse the decision of the Examiner rejecting these claims.

Respectfully submitted,

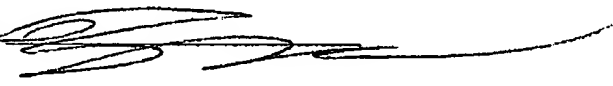
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Date: 2/17/06

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Trevor Lind, Reg. No. 54,785 

1055_Second Appeal Brief.wpd

IX. CLAIMS APPENDIX (37 C.F.R. §41.37(c)(1)(viii))

1. An electronic circuit adapted to send a signal to two or more separate electronic circuits over a common transmission line while simultaneously receiving signals from the two or more separate electronic circuits over the common transmission line, the electronic circuit comprising:
 - (a) signal sending circuitry coupled to an interface node which is adapted to be coupled to the common transmission line, the signal sending circuitry creating a combined signal at the interface node, the combined signal being dependent on the signal from the electronic circuit and the signals simultaneously applied by the two or more separate electronic circuits connected at other points to the common transmission line; and
 - (b) decoding circuitry coupled to the interface node, the decoding circuitry detecting the combined signal at the interface node and decoding the signals from the two or more separate electronic circuits responsive to the combined signal.
2. The electronic circuit of Claim 1 wherein the signal sending circuitry comprises:
 - (a) a signal driver; and
 - (b) an encoding element connected between the signal driver and the interface node.
3. The electronic circuit of Claim 2 wherein the encoding element comprises a resistor.

1 4. The electronic circuit of Claim 1 wherein the decoding circuitry comprises:

- 2 (a) a first differential receiver having a positive input connected to receive the
3 combined signal and having a negative input connected to a first reference voltage
4 source.

5
6 5. The electronic circuit of Claim 1 wherein the decoding circuitry comprises:

- 7 (a) a reference voltage multiplexer connected to receive a first digital signal as a
8 control signal, and having second and third reference voltage inputs;

- 9 (b) a second differential receiver having a positive input connected to receive the
10 combined signal, and a negative input connected to receive an output of the
11 reference voltage multiplexer.

12
13 6. The electronic circuit of Claim 1 wherein the decoding circuitry comprises:

- 14 (a) an additional reference voltage multiplexer connected to be controlled by a first
15 digital signal and a second digital signal and having fourth, fifth, sixth, and
16 seventh reference voltage inputs; and

- 17 (b) a third differential receiver having a positive input connected to receive the
18 combined signal and a negative input connected to receive an output from the
19 additional reference voltage multiplexer.

1 7. An electronic circuit arrangement comprising:

2 (a) three or more circuits connected together by a common transmission line, each
3 circuit adapted to assert a respective digital signal;

4 (b) each circuit including sending circuitry connected to the common transmission
5 line, the sending circuitry of the respective circuits cooperating to produce an
6 encoded signal on the transmission line based upon the values of the respective
7 digital signals asserted by the respective circuits, the encoded signal comprising
8 one signal from a set of unique encoded signals with each different signal in the
9 set being representative of a particular combination of digital signals asserted
10 simultaneously from the respective circuits; and

11 (c) each circuit further including a decoding arrangement for decoding the encoded
12 signal appearing on the common transmission line to produce the digital signals
13 asserted from each other circuit.

14
15 8. The electronic circuit arrangement of Claim 7 wherein each circuit is located on a
16 separate integrated circuit chip and the common transmission line comprises a conductor
17 connected to a single electrode on each separate integrated circuit chip.

18
19 9. The electronic circuit arrangement of Claim 7 wherein the signal sending circuitry in each
20 respective circuit includes an encoding element comprising a resistor.

1 10. The electronic circuit arrangement of Claim 7 wherein the three or more circuits includes
2 a first circuit providing a first digital signal, a second circuit providing a second digital
3 signal, and a third circuit providing a third digital signal, and wherein the decoding
4 arrangement associated with the second and third circuits includes a first digital signal
5 decoding arrangement comprising:

6 (a) a first differential receiver having a positive input connected to receive the
7 encoded signal and having a negative input connected to a first reference voltage
8 source.

9
10 11. The electronic circuit arrangement of Claim 7 wherein the three or more circuits includes
11 a first circuit providing a first digital signal, a second circuit providing a second digital
12 signal, and a third circuit providing a third digital signal, and wherein the decoding
13 arrangement associated with the first and third circuits includes a second digital signal
14 decoding arrangement comprising:

15 (a) a reference voltage multiplexer connected to receive the first digital signal as a
16 control signal, and having second and third reference voltage inputs;

17 (b) a second differential receiver having a positive input connected to receive the
18 encoded signal, and a negative input connected to receive an output of the
19 reference voltage multiplexer.

20
21 12. The electronic circuit arrangement of Claim 7 wherein the three or more circuits includes
22 a first circuit providing a first digital signal, a second circuit providing a second digital

1 signal, and a third circuit providing a third digital signal, and wherein the decoding
2 arrangement associated with the first and second circuits includes a third digital signal
3 decoding arrangement comprising:

- 4 (a) an additional reference multiplexer connected to be controlled by the first digital
5 signal and second digital signal, and having fourth, fifth, sixth, and seventh
6 reference voltage inputs; and
7 (b) a third differential receiver having a positive input connected to receive the
8 encoded signal and a negative input connected to receive an output from the
9 additional reference voltage multiplexer.

10
11 13. An electronic system having a first circuit producing a first digital signal, a second circuit
12 producing a second digital signal, and a third circuit producing a third digital signal, the
13 system comprising:

- 14 (a) a first circuit encoding element included in the first circuit, a second circuit
15 encoding element included in the second circuit, and a third circuit encoding
16 element included in the third circuit, each respective encoding element connected
17 between a digital signal output of the respective circuit and a common
18 transmission network between the first, second, and third circuits, the first,
19 second, and third encoding elements cooperating to produce an encoded signal on
20 the common transmission network based upon the values of the first, second, and
21 third digital signals, the encoded signal comprising one signal from a set of unique

1 encoded signals with each different signal in the set being representative of a
2 particular combination of the first, second, and third digital signals; and

- 3 (b) a first circuit decoding arrangement included with the first circuit, a second circuit
4 decoding arrangement included with the second circuit, and a third circuit
5 decoding arrangement included with the third circuit, the respective decoding
6 arrangement for each respective circuit for decoding the encoded signal to
7 produce the digital signals produced by each other circuit in the system.
8

9 14. The electronic system of Claim 13 wherein the encoding elements each comprise a
10 resistor.
11

12 15. The electronic system of Claim 13 wherein the first circuit decoding arrangement
13 comprises:

- 14 (a) a reference voltage multiplexer connected to be controlled by the first digital
15 signal and connected to receive second and third reference voltage signals as
16 inputs;
17 (b) a second differential receiver having a positive input connected to receive the
18 encoded signal and a negative input connected to receive a reference voltage
19 multiplexer output;
20 (c) an additional reference voltage multiplexer connected to be controlled by the first
21 digital signal and the second digital signal, and connected to receive fourth, fifth,
22 sixth, and seventh reference voltage signals as inputs; and

1 (d) a third differential receiver having a positive input connected to receive the
2 encoded signal and a negative input connected to receive an output of the
3 additional reference voltage multiplexer.
4

5 16. The electronic system of Claim 13 wherein the second circuit decoding arrangement
6 comprises:

7 (a) a first differential receiver having a positive input connected to receive the
8 encoded signal and a negative input connected to receive a first reference voltage
9 signal;

10 (b) an additional reference voltage multiplexer connected to be controlled by the first
11 digital signal and the second digital signal, and connected to receive fourth, fifth,
12 sixth, and seventh reference voltage signals as inputs; and

13 (c) a third differential receiver having a positive input connected to receive the
14 encoded signal and a negative input connected to receive an output of the
15 additional reference voltage multiplexer.
16

17 18. The electronic system of Claim 13 wherein the third circuit decoding arrangement
18 comprises:

19 (a) a first differential receiver having a positive input connected to receive the
20 encoded signal and a negative input connected to receive a first reference voltage
21 signal;

- 1 (b) a reference voltage multiplexer connected to be controlled by the first digital
- 2 signal and connected to receive second and third reference voltage signals as
- 3 inputs; and
- 4 (c) a second differential receiver having a positive input connected to receive the
- 5 encoded signal and a negative input connected to receive an output of the
- 6 reference voltage multiplexer.

X. EVIDENCE APPENDIX (37 C.F.R. §41.37(c)(1)(ix))

The Appellants have not relied upon any evidence in this appeal according to 37 C.F.R. §41.37(c)(1)(ix) in order to overcome the currently outstanding grounds of rejection in the case.

- 1 **XI. RELATED PROCEEDINGS APPENDIX (37 C.F.R. §41.37(c)(1)(x))**
- 2 There is no related Appeal or Interference before the United States Patent and Trademark
- 3 Office.

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